

**Internal Representation and Behavioural Synthesis
of Control Dominated Applications (1996)** ([Make
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Hemani ESD Lab, Dept. ...



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Abstract: In this paper we address problems encountered in behavioural synthesis of control dominated applications that are common in telecommunications. An internal representation, optimized for capturing control dominated behaviours and a synthesis strategy that takes into account the control flow is presented. Results of applying this strategy to realistic examples is presented and compared to commercial behavioural synthesis tools. 1. Introduction There are several applications which require ASICs... ([Update](#))

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.... **how to map process structures from SDL into IRSYD [12] as well as a conceptual work for the internal representation of control flows [4].** Our intent is to present a generic mapping scheme to convert communication constructs from external languages into IRSYD in a consistent...

...proposed evolution of the AKKA design flow to AKKA, described in figure 32. **AKKA will use a graph based internal representation, XFC [29], to improve the hardware efficiency, estimations, and interface synthesis.** VHDL will be added as a front end language. FIGURE 33....

Cited by: [More](#)

ProGram: A Grammar-Based Method for Specification and Hardware.. - Öberg (1999) ([Correct](#))

Hardware/Software Partitioning of Telecommunication Systems - O'Nils (1996) ([Correct](#))

A Generic Scheme for Communication Representation and.. - Meincke, Jantsch.. (1999) ([Correct](#))

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3: Specification and Design of Embedded Systems (context) - Gajski, Vahid et al. - 1994

2: SOLAR: An Intermediate Format for System-Level Modelling and Synthesis (context) - Jerraya, O'Brien - 1994

2: IRSYD: An Internal Representation for Heterogeneous Embedded Systems - Ellervee, Kumar et al. - 1998

BibTeX entry: ([Update](#))

P. Ellervee, A. Kumar, B. Svantesson, A. Hemani, "Internal Representation and Behavioural Synthesis of Control Dominated Applications". The 14th NORCHIP Conference, pp.142-149, Helsinki, Finland, Nov. 1996.
<http://citeseer.ist.psu.edu/ellervee96internal.html> [More](#)

```
@misc{ ellervee96internal,  
  author = "P. Ellervee and A. Kumar and B. Svantesson and A. Hemani",  
  title = "Internal Representation and Behavioural Synthesis of Control Dominated  
    Applications",  
  text = "P. Ellervee, A. Kumar, B. Svantesson, A. Hemani, Internal Representation  
    and Behavioural Synthesis of Control Dominated Applications. The 14th NORCHIP  
    Conference, pp.142-149, Helsinki, Finland, Nov. 1996.",  
  year = "1996",  
  url = "citeseer.ist.psu.edu/ellervee96internal.html" }
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- 206 High-Level Synthesis: Introduction to Chip and System Design (context) - Gajski, Dutt et al. - 1993
- 14 A Tree-Based Scheduling Algorithm for Control-Dominated Circ.. (context) - Huang, Jeang et al. - 1993
- 9 Digital Design: Principles & Practices (context) - Wakerly - 1994
- 8 An Automaton Model for Scheduling Constraints in Synchronous.. (context) - Takach, Wolf et al. - 1995
- 6 A Novel Allocation Strategy for Control and Memory Intensive.. (context) - Svantesson, Ellervee et al. - 1996
- 5 Synthesis Using Path-Based Scheduling: Algorithms and Exerci.. (context) - Camposano, Bergamaschi - 1990
- 4 Scheduling of Behavioural VHDL by Retiming Techniques (context) - Wehn, Biesenack et al. - 1994
- 3 Digital Circuits and Logic Design (context) - Lee - 1976
- 2 LSI Digital Devices on Programmable Matrix Structures (context) - Baranov, Sklyarov - 1986
- 1 Modelling and Synthesis of Operational and management System (context) - Svantesson, Hemani et al. - 1995

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[Design of a GSM Vocoder using SpecC Methodology - Gerstlauer, Zhao, Gajski \(1999\)](#) (Correct)
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encoder ASIC partition (Note: DataIn and DataOut **FSMD** for behaviors other than the 2nd Levinson-Durbin .38 50 Behavior prefilter **FSMD**.)

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www.ics.uci.edu/pub/cad/cadlab-trs/1999/TR-99-11.vocoder.ps.gz

[Internal Representation and Behavioural Synthesis of Control.. - Peeter Ellervee \(1996\)](#) (Correct)
 (2 citations)

using the well developed finite state machine (**FSM**) optimization techniques. Based on the ideas, as a finite state machine which can be handled by an **FSM**/logic synthesis tool. In this paper, we present an Figure 1. CMIST synthesis strategy Output **FSM** in **VHDL** /Verilog Extract Arithmetic Components Schedule /
www.ele.kth.se/ESD/doc/ar96/lrv/norchip.ps.gz

[A Tool Converting Finite State Machine to VHDL - Amr Abdel-Hamid Mohamed](#) (Correct)

Abstract Finite state machines (**FSM**) are a basic component in hardware design, they between inputs and outputs for sequential designs. **FSMs** can be represented graphically, which would help A Tool Converting Finite State Machine to **VHDL** Amr T. Abdel-Hamid, Mohamed Zaki and Sofi ene
www.ece.concordia.ca/~tahar/pub/CCECE04-FSM.pdf

[Automated Design of Finite State Machine Predictors - Timothy Sherwood Brad \(2001\)](#) (Correct)

Estimation Abstract Finite State Machines (**FSM**) are a fundamental building block in computer we present a framework for automated design of small **FSM** predictors for general purpose and customized expression is then converted into a **FSM**. The **VHDL** for synthesis is then generated from the **FSM**.
www.cse.ucsd.edu/~calder/papers/FSM.pdf

[comp.lang.vhdl Frequently Asked Questions And Answers.. - Preliminary Remarks This](#) (Correct)

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tech-www.informatik.uni-hamburg.de/vhdl/doc/faq/FAQ3.pdf

[BDDBased Testability Estimation of VHDL Designs - Ferrandi, Fummi, Macii.. \(1996\)](#) (Correct)

is described in **VHDL** as a network of interacting **FSMDs**. In addition# it is assumed that the testability usually speci#ed through a network of interacting **FSMs** #IFSM#In this sense# we can claim that the Euro-Dac '96 With Euro-**Vhdl** '96 0-89791-848-7/96 \$4.00 1996 IEEE Bdd#based
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[Automated Design of Finite State Machine Predictors for.. - Sherwood, Calder \(2001\)](#) (Correct)

shrinking design times. Finite State Machines (**FSM**) are a fundamental building block in computer we present a framework for automated design of small **FSM** predictors for customized processors. Our approach expression is then converted into a **FSM**. The **VHDL** for synthesis is then generated from the **FSM**.
www-cse.ucsd.edu/~calder/papers/ISCA-01-FSM.ps

[Application Specific Processor Synthesis from.. - Tammemäe, Udre..](#) (Correct)

by a finite state machine. Hence we use a **FSM** model as internal representation for state for state extraction and scheduling. The **FSM** is a Moore type automaton. The internal Processor Synthesis from Assembler Code using **VHDL** K. Tammemae, J. Udre Tallinn Technical University
www.ele.kth.se/%7Enalle/asiapap.ps.gz

Tools for mapping applications to CCMs - Mark Jones Michael (1998) (Correct)

inner product: A tree-structured graph with a small **FSM**, 4 adders and 4 multipliers The **FSM** is assigned to with a small **FSM**, 4 adders and 4 multipliers The **FSM** is assigned to the CPU and the adders/multipliers a DSP Select from a library or write from scratch **VHDL**, C, assembly, etc for each of the tasks (cells) www.ccm.ece.vt.edu/papers//spie2.pdf

A Dedicated Circuit for Charged Particles Simulation.. - Negoi, Guyot, Zimmermann (Correct)

Design of datapath architecture Design of operators **FSM** description (**VHDL**) and synthesis Processor architecture Design of operators **FSM** description (**VHDL**) and synthesis Processor description (structural and synthesis Processor description (structural **VHDL**) Validation **VHDL** simulation (logical gate level) verdon.imag.fr/pub/ISD/postscript/asap97.ps.gz

BDD-Based Testability Estimation of VHDL Designs - Ferrandi, Fummi, Macii.. (1996) (Correct)

is described in **VHDL** as a network of interacting **FSMDs**. In addition, it is assumed that the testability usually specified through a network of interacting **FSMs** (IFSM) In this sense, we can claim that the BDD-Based Testability Estimation of **VHDL** Designs Fabrizio Ferrandi Franco Fummi ipeca4.elet.polimi.it/pub/paper/ffm96c.ps.gz

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